Fast Parameter Extraction of General Interconnects Using Geometry Independent Measured Equation of Invariance

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***Abstract*— The measured equation of invariance (MEI) is a new concept in computational electromagnetics. It has been demonstrated that the MEI technique can be used to terminate the meshes very close to the object boundary and still strictly preserves the sparsity of the finite-difference (FD) equations. Therefore, the final system matrix encountered by the MEI is a sparse matrix with a size similar to that of integral equation methods. However complicated the Green's function, disagreeable Sommerfeld integrals, and very difficult umbilical meshes for multiconductors make the traditional MEI very difficult (if not impossible) to be applied to analyze multilayer and multiconductor interconnects. In this paper, the authors propose the geometry independent MEI (GIMEI) which substantially improves the original MEI method. The authors use GIMEI for capacitance extraction of general two-dimensional (2-D) and three-dimensional (3-D) very large scale integration (VLSI) interconnect. Numerical results are in good agreement with published data and those obtained by using FASTCAP from Massachusetts Institute of Technology (MIT) and some other commercial tools, while GIMEI's are generally an order of magnitude faster than FASTCAP with much less memory usage.**

***Index Terms*—Capacitance matrix, fast 3-D extraction, geometry independent, interconnects, measured equation of invariance (MEI), measuring loop.**

I. Introduction

THE DESIGN and development of next-generation electronic products is driven by an increasing demand for greater functionality, higher performance, and a shorter design-to-manufacturing cycle time in smaller, yet faster packaging. Currently, the feature size is as small as 0.35 μm, and it has been predicted in the *1994 National Technology Roadmap for Semiconductors (NTRS)* that the feature size will decrease to 0.25 μm in 1998, and 0.18 μm in 2001. Shrinking silicon geometries affects the electrical properties of the wires which produces a corresponding effect on the IC signals. As a result, factors which have an insignificant effect at 1 μm or larger become significant impediments to performance at 0.35 μm and smaller. One of the dominant factors affecting IC performance as feature size shrinks into deep submicron (less than 0.5 μm) is interconnect. Because transistor sizing is shrinking faster than the interconnect between transistors, wiring interconnects dominate the total gate-to-gate delay. For instance, at 2 μm, 80% delay is due to transistor or gate delay, and only 20% delay is attributed to the wires. In deep submicron design such as 0.25 μm and smaller, however, interconnect delay may account for some 80%–90% of the total delay for long nets. As interconnect becomes a principal determinant of performance, it is increasingly critical to both understand and account for its effects as part of the design process. This is done by modeling the interconnects and extracting parasitic parameters, which are effects not intentionally designed into the chip but are rather consequences of the layout. In the modeling, one has to consider the propagation delay and transmission line impedance, together with other effects such as signal degradation caused by transmission line dispersion, signal reflection at discontinuities, crosstalk between adjacent and cross lines, and simultaneous switching noise due to the inductance in power distribution system. And these effects must be quantified in order not to render a fabricated digital circuit inoperable or to distort an analog signal and make it fail to meet specifications. The current practice of modeling the interconnect with discrete components will not be accurate enough. In addition, nontrivial parasitic effects of nearby electrically different chip mask elements will also require greater detailed information and accuracy in modeling, including 3-D effects. Therefore, it is necessary to develop computationally efficient methods to extract the parasitics of the interconnects.

For an inhomogeneous structure like very large scale integration (VLSI) interconnects, the modes are hybrid and a full-wave approach should be adopted. However, the quasi-static (quasi-TEM) approximations are sufficiently accurate when the transverse components predominates over the longitudinal ones; in other words, the transverse dimensions of the structure are much smaller than the wavelength. Since the frequency range of interest for high-speed VLSI is often below 10 GHz, the quasi-TEM assumption is adopted. In fact, up to now the static capacitance matrix $[C]$ and inductance matrix $[L]$ of the multilayer and multiconductor interconnect is commonly used in practice for high-speed VLSI, printed circuit board (PCB), and multichip modules (MCM) design.

The various procedures to reach the solution can be generally classified into the following categories. One category is to solve differential Maxwell equations called domain or finite methods, such as the finite-element method (FEM) [1] and finite-difference method (FDM) [2], [3]. They basically divide the space surrounding the object into meshes, then write

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local equations at each mesh point, which leads to a sparse matrix system. But the standard FDM or FEM involves a large number of unknowns because of the fact that they get the solution of the potential distribution over the entire geometry domain and the boundary conditions are usually valid only far away from the object for open problem. Another category is using the integral equation approach such as method of moments (MoM) [4], the boundary-element method (BEM) [5], and the BEM with multipole acceleration [6]. They make meshes on the surface of the object. For multilayer, multiconductor interconnects, this means meshes are made either on the surface of each conductor with the Green's function for a layered medium which is both mathematically and computationally complex, or on the surfaces of each conductor and all dielectric interfaces but with the much simplified Green's function. Compared to FDM, this greatly reduces the number of unknowns; however, each small piece is either a source or field point, and are affected by all others, which leads to a full matrix. Therefore, all these methods will either solve a sparse but very large matrix or solve a small, but full, matrix. There is also another kind of semianalytical approach, such as the method of lines (MoL) [7], [8], spectral-domain approach (SDA) [9], and dimension-reduction technique (DRT) [10]. They basically take some special procedures and reduce the original problem by one dimension. The drawback of these methods is that the geometry they can deal with has some limitations. For example, MoL and SDA have difficulties to deal with nonzero thickness conductors, and it is hard to apply DRT to nonplanarized structures. Recently, several methods have been proposed to approach a sparse final matrix system whose number of unknowns is small. Among them, the measured equation of invariance (MEI), is one of the most natural and successful.

The MEI is a new concept in computational electromagnetics [11], [12]. MEI is used to derive the local finite-difference (FD) equation at a mesh boundary where the conventional FD approach fails. It is demonstrated that the MEI technique can be used to terminate the meshes very close to the object boundary and still strictly preserves the sparsity of the FD equations. Therefore, the final system matrix encountered by the MEI is a sparse matrix with size similar to that of integral equation methods, which results in dramatic savings in computing time and memory usage. The MEI has been applied to analyze microwave integrated circuits [13]–[15], to analyze scattering of penetrable medium problems [12], [16], to analyze scattering of anisotropic medium [17], and to analyze scattering in an open region combined with FEM's [18]–[21]. It has also been extended to time domain [22].

For multilayer and multiconductor structures, however, the deduction of the Green's function is very difficult. Also, the calculation of the MEI coefficients will encounter many Sommerfeld-type integrals. As a result, the calculation of MEI coefficients dominates the total computing time [15]. In addition, it becomes very difficult or inefficient to do an umbilical mesh as is done in a traditional MEI for a multiconductor system [13]–[15]. Therefore, the complicated Green's function, disagreeable Sommerfeld integrals, and a difficult mesh generation scheme make the traditional MEI very difficult, if not impossible, to be applied in analyzing multilayer and multiconductor interconnects.

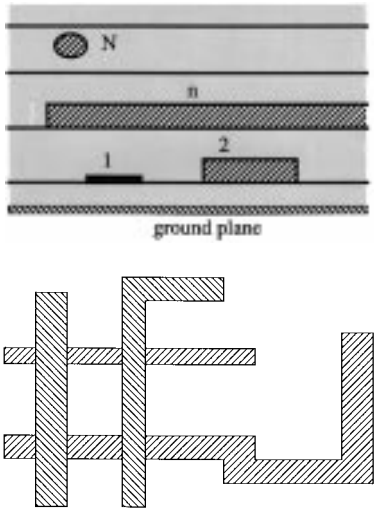

Fig. 1. A general 3-D interconnect configuration (the two figures are not related).

Recently, a MEI variety called geometry independent MEI (GIMEI) was proposed [23]–[25] which was verified as being very computationally efficient. GIMEI substantially improved the MEI in four key aspects by: 1) cancelling the postulate of geometry specific in the conventional MEI; 2) avoiding the deduction of the Green's function in a multilayer structure; 3) avoiding the calculation of disagreeable Sommerfeld-type integrals; and 4) avoiding the use of umbilical mesh. Using this method, the calculation of MEI coefficients only costs a very small part of the total computing time. Although by avoiding the Sommerfeld-type integral as the Green's function, this approach has a larger number of unknowns than traditional MEI procedures [13]–[15] and the overall efficiency is much better. In this paper, the authors extended the GIMEI to compute the capacitance matrix of general interconnects. The results are in good agreement with published data and those obtained by using FASTCAP from MIT [6]. Also, the GIMEI can generally achieve an order of magnitude faster than FASTCAP with significantly less memory usage.

This paper is organized as follows. Section II defines the problem. Section III briefly reviews the MEI method. Section IV describes the basic principle of the GIMEI. Section V gives several numerical and experimental results to verify the accuracy and efficiency of the GIMEI. Section VI presents the authors' conclusions.

II. Problem Formulation

A general interconnect configuration is shown in Fig. 1. For an N-conductor system, an $N \times N$ capacitance matrix is defined by

$$Q_i = C_{ii}\Phi_i + \sum_{j=1}^{N} C_{ij}(\Phi_i - \Phi_j), \qquad i = 1, 2, \cdots, N \quad (1)$$

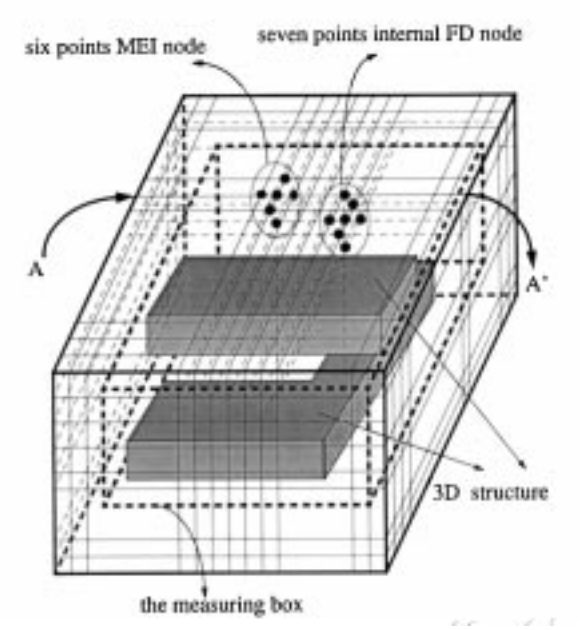

Fig. 2. Discretization mesh of a 3-D structure.

which can be rewritten as

$$Q_i = \sum_{j=1}^{N} C_{ij}^{s} \Phi_j, \qquad i = 1, 2, \cdots, N \tag{2}$$

where C_{ij}^{s} is the short circuit capacitance. In this paper, when talking about capacitance, the authors refer to the short circuit capacitance. Note that for a two-dimensional (2-D) case, the capacitance value is with respect to per-unit length. Now, the parasitic capacitance problem to be considered is reduced to the determination of the charge on each conductor for the known potentials.

The authors first discretize the geometry in interest into elementary boxes using a orthogonal Cartesian grid shown in Fig. 2. A 2-D case can be similarly derived [23]. The electrical potential can be assumed to be constant inside the elementary boxes and confined at the middle of the box. The mesh points on the metallization can be treated to be at a constant potential under the quasi-TEM assumption. The boundary of the mesh is treated later when the authors present the concept of the MEI.

The electrical potential function ϕ in the bounded region, except those mesh points on conductors of the quasi-static problem, satisfies the following Laplace equation:

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} + \frac{\partial^2 \phi}{\partial z^2} = 0. \tag{3}$$

Using difference to approximate derivative, one can write the electric potential at each internal mesh point as the linear combination of potentials of neighboring mesh points. By using the concept of a loop integral [12], one has derived a generalized local FD equation which can account for different step size and material along all directions with the error of $O(h^p), p \geq 1$, where $h = \max(h_x, h_y, h_z)$ [26].

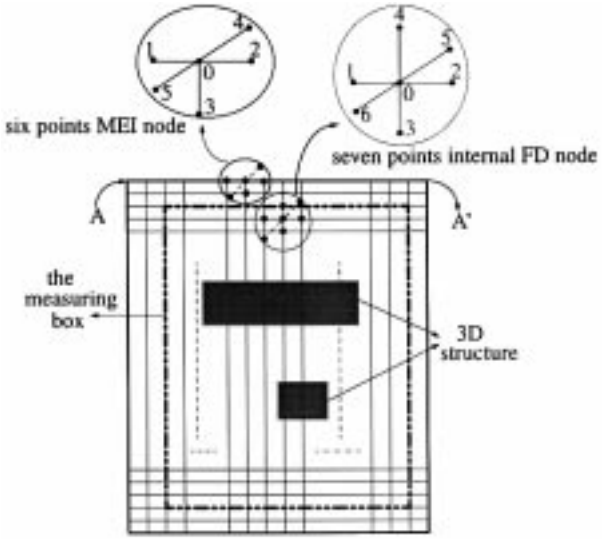

Fig. 3. A slice cut from Fig. 2 illustrating a measuring box.

III. Measured Equation of Invariance

The derived FD equation is only applicable at interior nodes of the mesh. In [11], Mei postulated that the FD/element equations at the mesh boundary points can also be represented by a local linear equation of the type

$$\sum_{i=0}^{M} C_i \phi_i = 0 \tag{4}$$

where M is the number of nodes that surrounding the node in interest ϕ_0. The node configuration is shown in Fig. 3 which is a slice cut from Fig. 2 with the surfaces A and $A\prime$. And the coefficients in (4) are: 1) location dependent; 2) geometric specific; and 3) invariant to the excitation. Equation (4) is called the MEI, and C_i, $i = 0, \cdots, M$, the coefficients of the MEI.

In a conventional MEI, the MEI coefficients are obtained by first setting a set of distribution functions, called *metrons* on conductors, then forming a linear algebraic equations with each element being the response of one certain metron at each boundary MEI node, and finally solving this linear equation. Then, the potential values at all nodes can be obtained by solving equations consisting of FD equations at interior nodes and the MEI at truncated mesh boundary nodes. The coefficient matrix of the system of linear algebraic equations is a sparse matrix since each row contains either seven nonzero elements from FD equations or M (or less) nonzero elements from the MEI. Here, M is at most six without considering diagonal nodes. It results in great savings in memory needs compared with the BEM or the MoM, etc. Furthermore, the computing time for a sparse matrix is greatly less than a dense matrix with similar dimension. The order of a coefficient matrix in the MEI approach is much less than that in conventional FDM's with absorbing boundary conditions, because the MEI can terminate the mesh very close to the region of interest here. These properties make the method of the MEI a powerful tool for computational electromagnetics.

Although some papers [27], [28] proposed some doubts on the third postulation of the MEI coefficients—invariant to excitations—these authors still admit in their papers that the MEI is an efficient technique for the truncation of mesh boundaries. Actually, their arguments were either not correct [29], [30] or did not conflict with the fundamentals of the MEI because it has already been proven that MEI coefficients are actually not strictly invariant to excitations, but instead are invariant to excitations with the error bounded by $O(h^2)$, where $h = \max(h_x, h_y, h_z)$ [31]. As stated above, the local FD equation also has the error of $O(h^p), p \geq 1$, therefore, the total truncation/model error of the final matrix system has the order of $O(h^p), p \geq 1$, which is not degenerated by the introduction of MEI equations on boundaries. The wide application of the MEI concept in computational electromagnetics has also contributed to the verification of the MEI's efficiency.

However, the closed-form Green's functions for multilayer structures of VLSI interconnects are generally derived in a spectral domain and then transformed to the space domain by inverse Fourier transformation that are infinite integrals. In addition to the tedious deduction of the Green's function in a multilayer structure, the calculation of the MEI coefficients is very time-consuming because many Sommerfeld-type integrals will be encountered. The calculation of MEI coefficients dominates the total computation time. As reported in [15], for a one-layer microstrip stub, obtaining the MEI coefficients required 90 central processing unit (CPU) min for a single frequency, and solving the sparse system required 24 min on a Dec Station 5000 series 200. On the other hand, in the traditional MEI, a umbilical mesh is adopted for coupled microstrip lines analysis [13]; however, this mesh generation scheme becomes extremely difficult to implement for multiconductor systems. Therefore, the complicated Green's function, disagreeable Sommerfeld-type integrals, and a very difficult mesh generation scheme make the MEI very difficult, if not impossible, to be applied to multilayer and multiconductor interconnects.

IV. Geometry Independent Measured Equation of Invariance

In order to overcome these drawbacks and apply this efficient truncation boundary concept in multiconductor, multilayer interconnects analysis, the authors introduced the measuring box concept, which is first proposed in [12] and further extended and explored in [23], [24]. A measuring box is just a closed surface that encloses all objects inside as shown in Figs. 2 and 3, to isolate the MEI nodes (boundary and the next layer) and possibly some buffer layers from the region containing conductors. In [23], it has been demonstrated that the MEI are also independent of the source distribution on the measuring loop provided the third postulate [31] MEI are independent of the source distribution on the conductors' surface. The MEI coefficients are then determined from the metrons on the measuring loop instead of the metrons on the conductors, which means that the MEI are independent of the geometries of the conductors or structure configuration. In order to avoid the Green's function in a multilayer structure, the dielectric layers are truncated at the measuring loop with physical polish which ensures such truncation will not affect the total accuracy; therefore, free space out of the measuring loop is assumed. Thus, the very simple free-space Green's function to measure the MEI coefficients can be used. Experiments suggest that very few layer meshes between the measuring loop and the nearest conductors, and very few layer meshes outside the measuring loop, are sufficient to guarantee the accuracy of these results in practice.

The potential values $\phi_i^k, i = 0, \cdots, M$, at the corresponding MEI nodes corresponding to the kth metron σ^k defined on the measuring loop can be simply obtained:

$$\phi_i^k = \int_{\Gamma_e} \sigma^k(s')\, G(\vec{r}_i, \vec{r}')ds', \qquad i=0,\cdots,M;\ k=1,\cdots,K \tag{5}$$

where Γ_e stands for the measuring loop, $\vec{r}_i, \vec{r}'$ denote the position vectors at the ith MEI node and the measuring loop, respectively, and K is the number of metrons. The 3-D quasi-static Green's function of free space is simply

$$G(\vec{r}_i, \vec{r}') = \frac{1}{4\pi|\vec{r}_i - \vec{r}'|} - \frac{1}{4\pi|\vec{r}_i - \vec{r}''|} \tag{6}$$

where $\vec{r}''$ is the image position vector of $\vec{r}'$ with respect to the ground plane, if any.

Substituting the potential values ϕ_i^k produced by the kth metron into the MEI (4), yields

$$\sum_{i=0}^{M} C_i \phi_i^k = 0, \qquad k = 1, 2, \cdots, K \tag{7}$$

which is a system of linear algebraic equations with respect to the MEI coefficients $C_1, C_2, \cdots, C_M$, when C_0 is normalized to 1. If the number of equations or the number of metrons is greater than M, one can solve (7) by least square techniques.

Generally, in a 3-D case, since global continuous metrons are difficult to find, the point metrons are selected and clustering techniques are adopted. Because under quasi-static assumption, only the amplitude information (no phase information compared with full-wave approach) is needed in the determination of the MEI coefficients, clustering is an efficient approximation. In this program, the CPU time to obtain the MEI coefficients are much less than solving the final sparse matrix, which means the overhead time spent on the MEI coefficients is only a very small part (less than 5%) of the total computing time.

Coupling the MEI equations at truncated mesh boundary nodes to the FD equations at interior nodes results in the matrix equation

$$[S]\,\bar{\phi} = \bar{f} \tag{8}$$

where $\bar{\phi}$ is a column matrix consisting of the potential values at all mesh nodes, and $\bar{f}$ is the known column matrix followed from the neighboring FD's around the conductors on which voltages are impressed.

From the solution of (8), one gets the potential distribution over the mesh region. Since the FD approximation of the Laplace equation is less accurate in the vicinity of a conductor's reentrant corner (i.e., a corner whose outside angle

is greater than π radians) because of a singularity in the electric field in the corner, one uses Duncan's correction [32] to get charge distribution or total charge on each conductor. Bringing these charges into (2), one can get the final short circuit capacitance matrix.

An adaptive mesh–remesh scheme has also been developed. In this scheme, the field is solved in a number of steps, the total computation time or solution accuracy is checked in each step, and whenever necessary the solution, including its accuracy information, is fed back to the mesh generator to further refine the mesh at the suitable location. This scheme makes the GIMEI field-solver flexible and time-bounded. Furthermore, this mesh generator can effectively treat arbitrary geometry including nonrectangular bends. This mesh emphasizes the location requiring higher resolution in a much more efficient way, resulting in much fewer mesh points and, hence, greater efficiency in the field-solver.

V. Experimental Results

It has been demonstrated by experimental results that the authors' approach is faster than the BEM (with multipole acceleration), MoM, and FD, without loss of accuracy. In addition, this method outperforms other methods mentioned above for fairly large structures. Furthermore, this method can be easily applied to structures with arbitrarily shaped cross-section conductors including infinitesimally thin conductors on lossy and inhomogeneous dielectric layers due to the nature of the FD used inside the measuring loop. To verify the accuracy and speedup advantage of this method, the following examples were selected to provide a quantitative measure. All relevant programs are run on a Sun Sparc 20 workstation.

A. 2-D Examples

Because the capacitance and inductance per-unit length do not vary when the whole geometry is scaled in a 2-D case, relative size of each configuration is given without specifying the units in the following examples.

1) A Thin Microstrip: The first example shown is an infinitesimally thin microstrip as in Fig. 4. The characteristic impedance Z_0 of this structure can be defined as $Z_0 = 1/(v_0\sqrt{CC_0})$ where v_0 is the speed of light in free space, C is the capacitance of this structure, and C_0 is the capacitance with the dielectric layer replaced by free space.

Fig. 5 shows the comparison of the characteristic impedance varying with the width–height ratio W/H obtained by using the GIMEI, Cao's result [4] which uses the MoM, Zutter's results [9] which are based on the space-domain Green's function approach (SDGA), and those provided by [33] and [34]. In the results of this paper, the authors use ten mesh points per-unit length. The difference of these results are within 2.5% compared with the results in [34] which is regarded as a standard reference for this kind of problem.

2) Two Coupled Microstrips: The second 2-D example is a pair of coupled microstrips touching a dielectric slab over a conducting plane as shown in Fig. 6. The conductors are numbered from left to right as 1 and 2, respectively. Table I compares these results with those of Cao's [4] and Weeks' [35]. For comparison, the results of [35] have been changed to dimension farads per meter. The differences are within 2.5%.

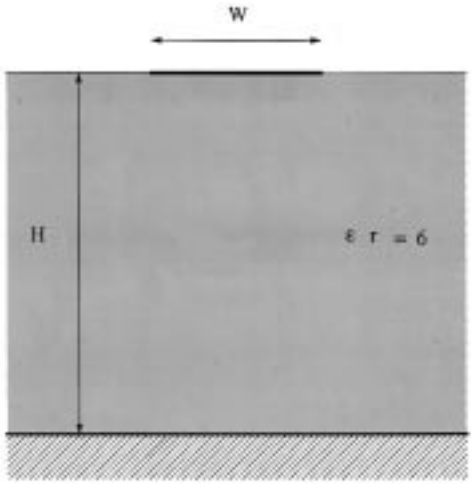

Fig. 4. A thin microstrip line.

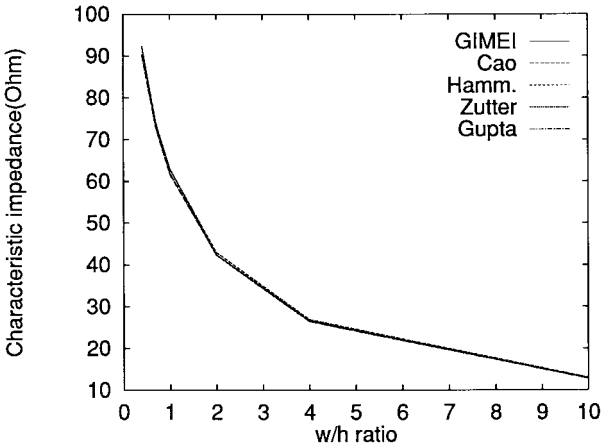

Fig. 5. Characteristic impedances Z_0 in ohms.

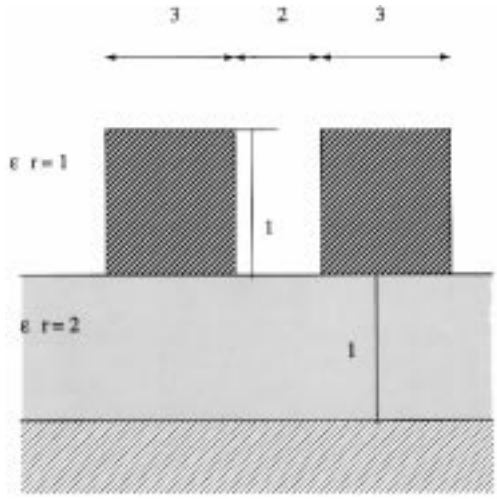

Fig. 6. Structure of coupled microstrips.

3) Three Lines with Three Dielectric Layers: A slightly more complex example is illustrated in Fig. 7. Table II shows

TABLE I
CAPACITANCE IN PF/M FOR FIG. 6

	GIMEI	Cao [4]	Weeks [35]
C11	93.80	91.65	92.24
C12	-8.322	-8.220	-8.504
C21	-8.322	-8.220	-8.504
C22	93.80	91.65	92.24

TABLE II
CAPACITANCE IN PF/M FOR FIG. 7

	GIMEI	Zutter [9]
C11	144.21	142.09
C12	-22.95	-21.733
C13	-0.129	-0.892
C21	-23.43	-21.733
C22	97.248	93.529
C23	-20.583	-18.098
C31	-0.126	-0.890
C32	-20.202	-18.097
C33	87.649	87.962

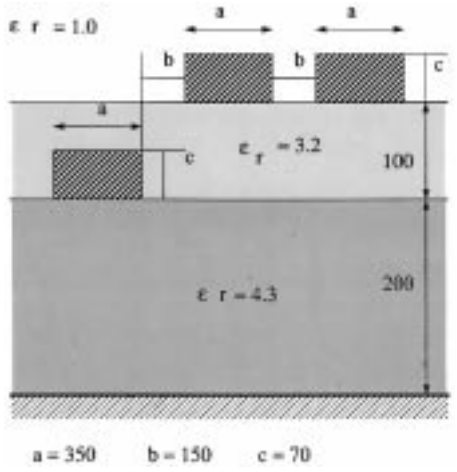

Fig. 7. Configuration of three line bus in layered dielectric.

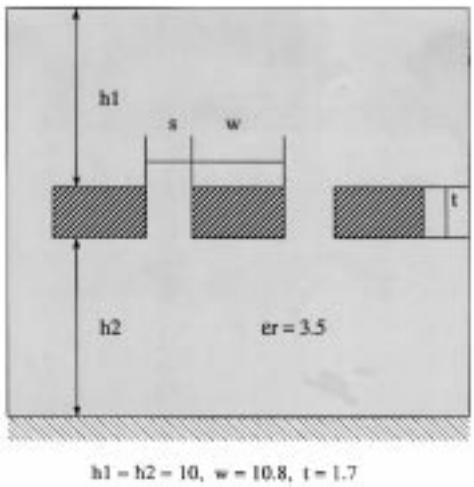

Fig. 8. Three parallel wires immersed in a dielectric.

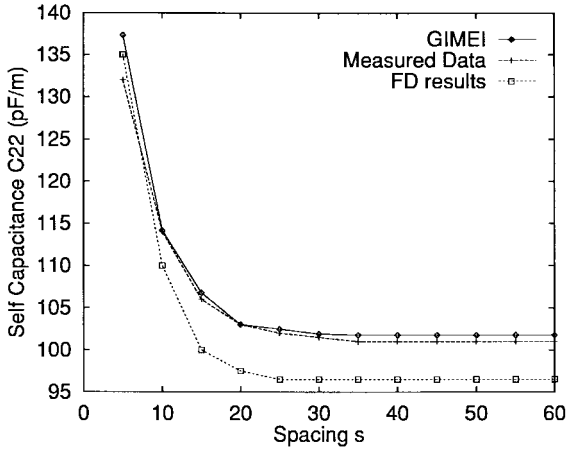

Fig. 9. C22 versus the interwire distances for Fig. 8.

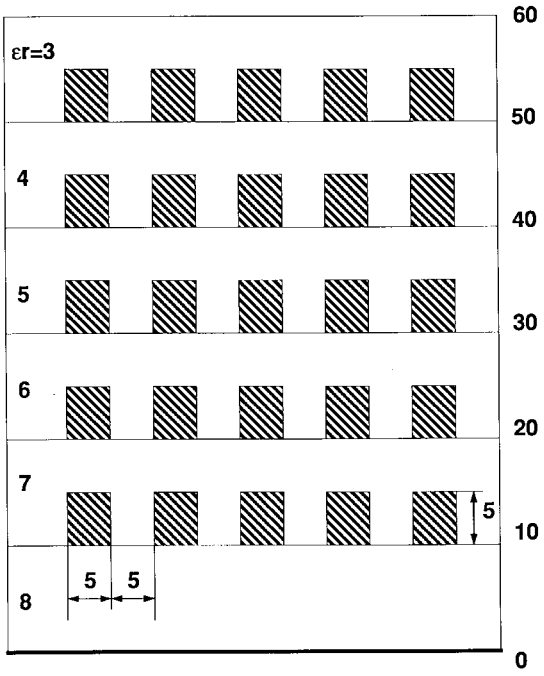

Fig. 10. Example of a configuration of 12 lines.

TABLE III
SELF CAPACITANCE IN PF/M FOR FIG. 10

Cond. #	GIMEI	BEM
1	322.8	316.2
2	366.7	391.5
3	325.2	316.5
4	307.9	309.5
5	344.1	364.1
6	309.0	309.5
7	258.1	260.5
8	289.3	306.1
9	258.7	260.5
10	165.3	161.9
11	203.0	214.7
12	165.7	161.9

these results together with the comparison with those of [9]. Here the conductors are numbered from left to right as 1, 2, and 3, respectively.

TABLE IV
SELF CAPACITANCES IN AF($10^{-18}F$) OF THE CUBE AND THE CPU TIME IN SECONDS

cubes in μm	GIMEI results	FASTCAP results	difference percent	GIMEI CPU time	FASTCAP CPU time	CPU time $\frac{FASTCAP}{GIMEI}$
1x1x1	73.89	73.38	0.7%	0.21	0.7	3.3
1x1x3	114.8	115	0.2%	0.29	1.9	6.6
1x1x5	149.8	149.6	0.1%	0.34	3.6	10.6
1x1x8	196.4	196.2	0.1%	0.45	4.7	10.4
1x1x10	225.4	225	0.2%	0.52	6.8	13.1

TABLE V
CAPACITANCE IN AF AND CPU TIME IN SECOND OF $1 \times 1 \times 5\mu$m CUBE USING E.W. BOUNDARY CONDITION

buffer #	C (aF)	CPU time	matrix order
3	241.6	0.25	1,000
5	197	1.89	5,000
10	174	9.1	20,000
15	164	28.67	50,000
20	159.4	68.45	100,000
25	155	146.76	200,000
30	151	250.58	300,000

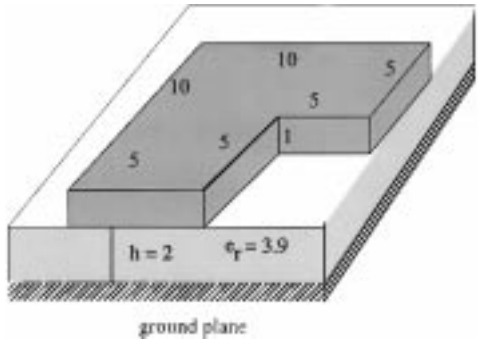

Fig. 11. A right-angle bend over a ground plane.

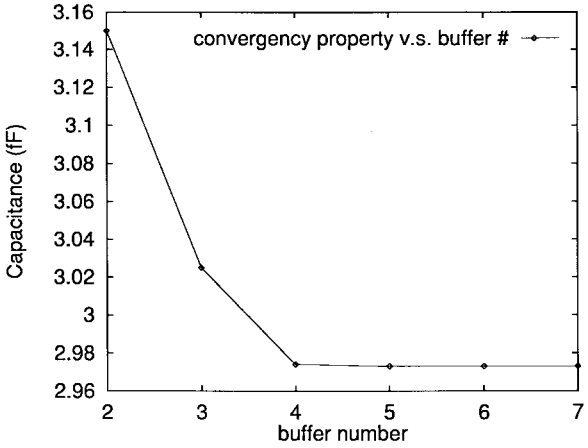

Fig. 12. Self-capacitance versus buffer number.

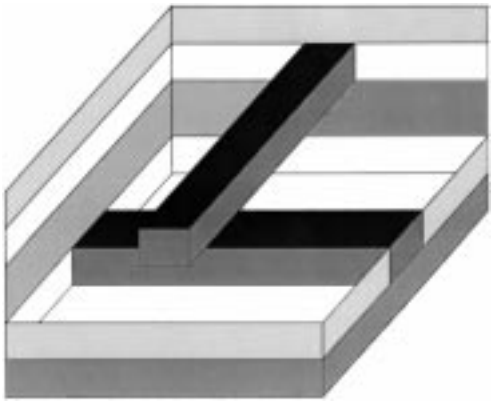

Fig. 13. A 1×1 cross over a ground plane.

4) Three Parallel Lines Immersed in Dielectric Compared with Measured Data: This example, whose configuration is shown in Fig. 8, shows three parallel wires immersed in a dielectric which is a commonly found structure in microelectronics. The structure represents three equidistant rectangular wires running parallel to a ground plane, where each conductor has the same size $w \times t$, and the space s varies from 5 to 60. This structure has been measured by Lin [36]. Fig. 9 shows capacitance of the middle conductor $C22$ varying with the interwire distance. A difference of less than 3% is observed in the whole range between the authors' results and the measured data [36]. It's clear from the figure that the authors' results are closer to the measured data than those obtained by a commercial 3-D interconnect modeling tool using the FDM.

5) A Large Multilayer and Multiconductor Example: To show that the authors' method is a very fast parameter extractor, an artificial example is given below. Here, for the sake of convenience, although the authors' method can handle arbitrarily shaped cross-section structures, only regular shaped cross-section structures are used. The example shows five dielectric layers and 12 conductors shown in Fig. 10. The conductors are numbered in sequence from left to right and from bottom to top. All conductors have the size of 5×5 and the spacing between the two adjacent conductors on the same layer is also 5. The outer space is all free space with $\varepsilon_r = 1$.

Table III shows the comparison of the authors' results and those computed by the BEM. A difference of approximately 5% is observed. Because the capacitance matrices are fairly big (12×12), the authors only give the results of self capacitances of each conductors. The authors' method, which takes 5.5-s CPU time, is eight times faster than the BEM which takes 43.97-s CPU time. The differences are less than 5%.

B. 3-D Examples

The authors have also extended the GIMEI into a 3-D problem.

1) A Simple 3-D Example: Cube with Different Longitude in Air, Compared with FASTCAP as well as FD with Zero E-Field Boundary Condition: To verify the speedup and accuracy

TABLE VI
CAPACITANCE IN AF FOR $1 \times 1 \times z$ CROSSOVER PROBLEM

Conductor length z (μm)	C_{11} GIMEI	C_{11} FASTCAP	C_{22} GIMEI	C_{22} FASTCAP	C_{12} GIMEI	C_{12} FASTCAP
4	230	226	180.6	176	-61	-60.41
5	260	265	203.5	205	-66.5	-68.43
7	348.7	341.4	260.1	253.7	-80.1	-79
10	440.3	451.6	326.8	324.2	-86	-87

TABLE VII
COMPARISON OF CPU TIME IN SECONDS AND MEMORY IN MEGABYTES FOR CROSSOVER PROBLEM

Length z (μm)	GIMEI CPU time	FASTCAP CPU time	CPU time $\frac{FASTCAP}{GIMEI}$	GIMEI memory	FASTCAP memory	Memory Use $\frac{FASTCAP}{GIMEI}$
4	2.8	24.37	8.7	3.5	22	6.3
5	3.23	26.06	8.1	3.7	24.5	6.6
7	6.5	65.62	10.1	5.6	60	10.7
10	9.16	93.24	10.2	6.5	78	12

TABLE VIII
COMPARISON OF EXTRACTED CAPACITANCE IN fF AND MESH SIZE

Examples	BEM results	FD results	GIMEI results	FD grid #	GIMEI grid #	FD time (sec)	GIMEI time (sec)
11 metals	3.29	3.436	3.446	250k	45k	525	54
14 metals	2.08	2.479	2.573	250k	78k	558	70

property of the GIMEI, a simple example of a $1 \times 1 \times z$ cube (unit in μm) is computed and compared with FASTCAP [6], which basically uses the BEM with multipole acceleration. The cube computed is extended along one direction z. Table IV shows the results (self-capacitance of the cube varying with the extended edge z) and CPU time of the GIMEI compared with those of FASTCAP. The GIMEI is about ten times faster than FASTCAP with the difference in the results of less than 1%.

The authors have also compared their results with those of standard FD under the zero E-field (electric wall [E.W.]) boundary condition using the same mesh discretization. The structure is chosen to be a $1 \times 1 \times 5 - \mu$m cube. Table V shows the results by using an E.W. varying with the layer number outside the measuring loop. To achieve the results close enough to the accurate ones (149.8 aF from the GIMEI and 149.6 aF from FASTCAP), the FDM requires as many as 30 mesh layers outside the measuring box, referred to as buffer layers, and takes more than 250 s. On the other hand, the GIMEI only needs three buffer layers and takes 0.34 s.

2) Proper Buffer Number Selection in a Right-Angle Bend Example: A simple right-angle bend is shown in Fig. 11, where all dimensions are in μm.

While FASTCAP got the self-capacitance of the bend (2.956 fF) in 16.1 s, the GIMEI obtained the result (2.974 fF) in 1.16 s. Again in this case, the GIMEI is more than ten times faster than FASTCAP. It is worth noting that in [3], the result is 105 F which is unreasonable. Fig. 12 shows the capacitance obtained by the GIMEI varying with the buffer number outside the measuring loop. As indicated, one only needs to use four to five buffer layers to get enough accurate results.

3) A Series of 1×1 *Crossover:* Fig. 13 shows a 1×1 cross immersed in five dielectric layers with a ground plane at the very bottom of the structure. The structure parameters are as follows. The height of each dielectric layer is 1 μm. Each metal line has the width of 1 μm, and the two lines have the same length $z\mu$m. And they are overlapped both in the middle of the other line. The dielectric relative permittivities are all chosen to be 3.9 for the sake of simplicity. The lower metal is numbered one while the higher is numbered two.

Table VI shows the results of short circuit capacitances C_{11}, C_{22}, and C_{12} computed by both the GIMEI and FASTCAP varying with the line length z. They are within the difference of 3%. Table VII shows the CPU time and memory usage of the two methods. The number of buffer layers outside the measuring box for the GIMEI is three. The GIMEI uses an order of magnitude of less computing time and memory usage than FASTCAP.

4) 3-D Structures Cut from a Real Design: The authors have also compared their field-solver results with the BEM and FDM on two larger 3-D examples using five metal layer technology. The first example has 11 metal lines, while the second has 14 metals, with the metals distributing from M1 (metal 1) to M4 (metal 4), and include many crossovers. The results are shown in Table VIII.

It is clear that the GIMEI uses much less grid size than the FDM and, thus, much less computing time. Generally speaking, because meshes close to objects are truncated and still keep the sparsity of the final system matrix, the GIMEI can treat larger structures faster than other numerical methods.

VI. CONCLUSIONS

In this paper, by using the measuring loop, the authors substantially improved the MEI in four key aspects by: 1) cancelling the postulate of geometry specific in the conventional MEI; 2) avoiding the deduction of the Green's function in the multilayer structure; 3) avoiding the calculation of

disagreeable Sommerfeld-type integrals; and 4) avoiding the use of an umbilical mesh, but still keeping all the advantages of the MEI, and successfully introducing the concept of the MEI as an efficient truncation boundary condition into the analysis of 3-D interconnects. Using the GIMEI, the calculation of the MEI coefficients only costs a very small part of the total computing time. Numerical and experimental results show that the GIMEI proposed in this paper is generally an order of magnitude faster than FASTCAP using the BEM with multipole acceleration and other commercial tools without loss of accuracy. Furthermore, this technique can easily handle the interconnect problems with an arbitrarily shaped cross section and lossy and inhomogeneous dielectric media. The technique can also be extended to 2-D or 3-D dynamic analysis of multilayer multiconductor interconnect problems.

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